This research proposes the concept of energy proportional computing applied to Xilinx All Programmable SoCs to implement heterogeneous and reconfigurable processors. The run-time power gating approach is applied to Xilinx ZYNQ devices that incorporate a hardened Cortex A processor in a different power domain. This work leverages a software centric approach based on OpenCL for describing applications and a processor-centric platform such as Xilinx All Programmable SoCs to implement accelerators and mapping algorithms.

**High-Level Models should be:**
- Covers PL, PS and memories
- Simple
- Compositional
- Descriptive

**Specially the PL High-Level Models should:**
- Describes different hardware and software
- Describes different accelerator modes
- Idle
- Data transfer
- Active
- Computational

**ZYNQ (FPGA+ARM)**

The results show that the minimum time that the FPGA must remain in power-off state for the technique to be energy efficient is in the order of milliseconds and up to 98% power reduction occurs when the fabric voltage is lowered below critical level.